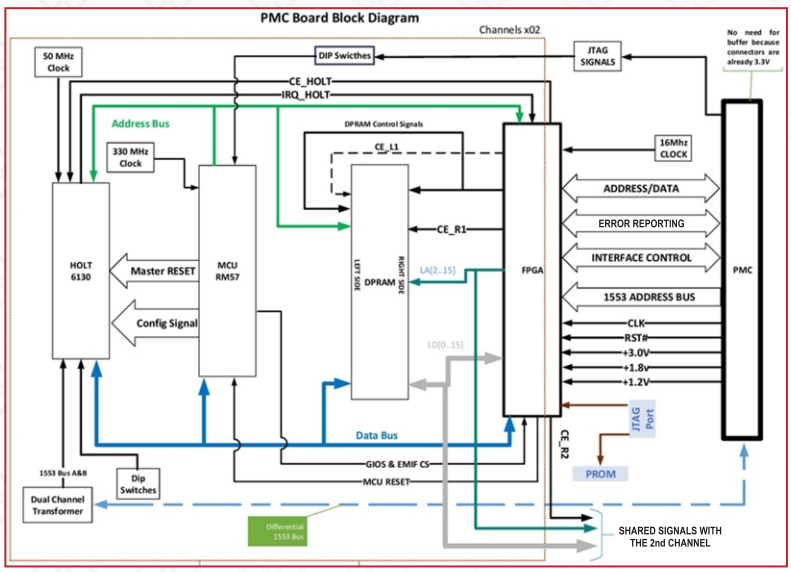
DATA SHEET

MUX BUS INTERFACE CARD

TERESOL
Technological Research Solutions

BLOCK DIAGRAM



Dual Channel MIL-STD-1553B PMC Interface Module

Specifications

Integrated Host Processor
- x02 ARM Cortex - R5F 32-Bit RISC CPU
- Dual-Core Lockstep CPUs With ECC-Protected Caches
- 1.66 DMIPS/MHz With 8-Stage Pipeline
- FPU With Single- and Double-Precision
- 16-Region Memory Protection Unit (MPU)
- 32KB of Instruction and 32KB of Data Caches With ECC

Random Access Memory
- x02 high-speed 16K x 16-bit Dual-Port Static RAM
- +3.3V Compatible IO Access

Flash Memory
- Low-Power AdvancedCMOS NOR Flash
- 40MbitPROM for FPGA

Mezzanine Slots
- One PMC slot for PCI@33Mhz

MIL-STD-1553 Interfaces
- x02 Independent dual redundant channels
- Multi-terminal Functionality
- Each channel functions as Bus Controller (BC), a Bus Monitor Terminal (MT) and two independent Remote Terminals (RTs).

Temperature Sensor
- x04 Processor Core Temperature sensors

Power Requirements
- Operates on +1.2V, +1.8V and +3.3V DC supply

Features

- Onboard Xilinx 6 Series high-end FPGA for AS ICs design
- High-speed 3.3V 16K x 16 dual-port SRAM
- 2x Mil-Std-1553 Differential Channels
- Standard PCI @33 MHZ Interface

Optional Accessories

- Temperature management

Standards

- MIL-STD-454G
- MIL-STD-8010
- MIL-STD-461B
- MIL-STD-1553B

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